REMARKS

In the Office Action, the Examiner indicated that claims 1 through 8 are pending in the application. The Examiner objected to claims 4, 5, 7, and 8 and rejected claims 1-3 and 6.

The Present Invention

The present invention relates to a hardware accelerator, e.g., as used in a DSP that is provided with a parameter RAM memory exclusively for storing data for populating variables of programming instructions for use in programming instructions stored elsewhere. An example of such variables are the parameters required for the various operating conditions of the accelerator. In a DSP application, the DSP can easily and without hardware modification accommodate design changes such as the need to support additional ADSL lines.

More particularly, in a preferred embodiment, the invention is a digital signal processor (DSP), comprising a hardware accelerator and a parameter RAM coupled to the hardware accelerator, the parameter RAM storing operating condition parameters for use by the hardware accelerator. In another preferred embodiment, the DSP is used in connection with a communication system employing plural ADSL lines, and the parameter RAM is configurable to store operating condition parameters for each of the plurality of ADSL lines.

U.S. Patent No. 6,704,871 to Kaplan et al.

U.S. Patent No. 6,704,871 to Kaplan et al. ("Kaplan") teaches a cryptographic co-processor. A secure communication platform on an integrated circuit is a highly integrated security processor which incorporates a general purpose DSP, along with a number of high performance cryptographic function elements, as well as a PCI and PCMCIA interface. The Examiner relies upon Kaplan for an alleged teaching of a DSP having a hardware accelerator and a parameter RAM coupled to the hardware accelerator, with the parameter RAM being adapted to exclusively store data for populating variables of programming instructions for use in programming instructions stored elsewhere and used by the hardware accelerator. The Examiner asserts that kernel RAM 32 is analogous to the claimed parameter RAM of the present invention; that the data for populating variables of programming instructions comprises a keyset; that programming instructions populated by the keyset comprise a secure kernel; and that the location of the programming instructions that are stored elsewhere comprises read-only memory (ROM).

U.S. Patent No. 5,883,907 to Hoekstra

U.S. Patent No. 5,883,907 to Hoekstra ("Hoekstra") teaches an asymmetrical digital subscriber line (ADSL) block encoder circuit and method of operation using a pipelined structure. The Examiner relies upon Hoekstra for an asserted teaching of a plurality of ADSL lines.

Claim Rejections, 35 U.S.C. §102

On page 2 of the Office Action, the Examiner rejected claims 1 and 2 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,704,871 to Kaplan et al. ("Kaplan").

In this response, applicant has amended claim 1 to include the limitations of claim 3, and added one additional element from allowable claim 4. Claim 3 has thus been canceled. This amendment renders the rejection under 35 U.S.C. §102 moot. Accordingly, the Examiner is respectfully requested to reconsider and with the rejection of claims 1 and 2 under 35 U.S.C. §102(e).

Rejection of Claims under 35 U.S.C. §103(a)

On page 3 of the Office Action, the Examiner rejected claims 3 and 6 under 35 U.S.C. §103(a) as being unpatentable over Kaplan in view of U.S. Patent No. 5,883,907 to Hoekstra ("Hoekstra"). As noted above, the substance of claim 3 is now included in claim 1. Thus, claims 1, 2 and 6 are now deemed by the Examiner to be obvious based on the combination of Kaplan and Hoekstra. This rejection is respectfully traversed.

The present claimed invention includes a parameter RAM coupled to a hardware accelerator. A parameter RAM is a specific type of RAM that simply saves data (parameters) pertaining to variables, not programming instructions. The parameters stored in the parameter RAM are used to populate variables in programming instructions that are stored somewhere other than in the parameter RAM. This allows the program instructions and control words to be hard-coded, thereby requiring less memory and thus consuming less space. As claimed in

claim 1, the combination of hardware accelerator and parameter RAM is used in a digital signal processor for use in a communication system employing plural ADSL lines. In accordance with the limitations of amended claim 1, the parameter RAM is selectively configurable to store operating condition parameters for each of said plurality of ADSL lines. Applicant directs the Examiner's attention to the fact that the term selectively did not appear in original claim 3. However, applicant notes that the selective configuration is claimed in allowable claim 4.

Kaplan is non-analogous art. Kaplan is directed to a cryptographic co-processor, whereby a secure communications platform is integrated with an off-the-shelf DSP so that a vendor who is interested in digital signal processing can also receive built-in security functions which cooperate with the DSP. This is far removed from the DSP of the present invention, which enables hard-coding of control words so that less memory is required and less space is consumed.

As stated in column 6, lines 57-60 of Kaplan, the co-processor of Kaplan "performs all of the functions of the conventional DSP but also has the unique capability of providing secure communications". The present invention as claimed has nothing whatsoever to do with providing secure communications. As noted in the specification, the special elements of the present invention are highlighted when combining a plurality of ADSL lines. Nothing in Kaplan teaches or suggests these features, features which are claimed in independent claim 1. The Examiner also acknowledges that Kaplan does not "show the plurality of ADSL lines as claimed."

The addition of Hoekstra does not provide the appropriate suggestion to combine the teachings of Kaplan with Hoekstra to achieve the claimed invention. Applicant does not deny that Hoekstra discloses a plurality of ADSL lines. Applicant does not claim to be the inventor of the use of a plurality of ADSL lines. Rather, applicant has invented a novel DSP that has specific beneficial results when used to store operating conditions for multiple ADSL lines. The mere "showing" of plural ADSL lines does not meet the test for obviousness under 35 U.S.C. §103. Nothing in Hoekstra, nor Kaplan teaches or suggests such a combination, and thus the test is not met.

It is noted that Kaplan's use of user mode and kernel mode, as described in column 6, lines 28-38, highlights a functional difference between the Kaplan invention and the claimed invention herein. Lines 33-34 of Kaplan state that in the user mode, the kernel space is not accessible, while in kernel mode it is accessible (and even then, only through a secure kernel firmware that the DSP must execute). This is different, operationally from the present invention and simply highlights the non-analogous nature of the Kaplan reference.

To summarize, the claimed invention is not taught or suggested by the combination of Kaplan and Hoekstra. Accordingly, the Examiner is respectfully requested to reconsider and withdraw the rejection based upon 35 U.S.C. §103.

Conclusion

All of the claims are in condition for allowance. Accordingly, reconsideration of the claims and an early Notice of Allowance are earnestly solicited.

The Commissioner is hereby authorized to charge any fees associated with this communication to Deposit Account No. 19-5425.

Respectfully submitted

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